METHOD OF ERASING NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE AND SUCH NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE

ABSTRACT OF THE DISCLOSURE

A method of erasing a non-volatile semiconductor memory device comprising, to raise the convergence of the erasure voltage, performing a write-erase operation, at least one write-erase operation after erasure, or a plurality of write-erase operations as an operation when erasing a memory transistor including dispersed charge storing means in a gate insulating film interposed between a channel-forming region of the semiconductor and a gate electrode and, to increase the erasure speed, optimizing an erasure voltage and/or an erasure time in accordance with the phenomenon of the absolute value of a voltage of an inflection point taking an extremum at the erasing side in a hysteresis curve shown the change of threshold voltage with respect to an applied voltage of the memory transistor becoming larger along with a shortening of a voltage application time.